CLC: Configurable Logic Cell

The Configurable Logic Cell (CLC) provides programmable logic that operates outside the speed limitations of software execution.

The logic cell takes up to 16 input signals and through the use of configurable gates reduces the 16 inputs to four logic lines that drive one of eight selectable single-output logic functions.

Input sources are a combination of the following:

- I/O pins
- Internal clocks
- Peripherals
- Register bits

The output can be directed internally to peripherals and to an output pin.
Possible configurations include:

- Combinatorial Logic
  - AND
  - NAND
  - AND-OR
  - AND-OR-INVERT
  - OR-XOR
  - OR-XNOR
- Latches
  - S-R
  - Clocked D with Set and Reset
  - TransparentDwithSetandReset
  - Clocked J-K with Reset

CLC Video Tutorial This video introduces the Configurable Logic Cell (CLC) for Microchip 8-bit MCU devices and shows how to use it.

https://www.youtube.com/watch?v=rNE1sl21x5M&feature=youtu.be >> https://youtu.be/rNE1sl21x5M

CLC Setup

The CLC peripheral has four sections that need to be setup before it can be used.
This involves setting up 8 registers in your software program.
Once these registers are setup, the CLC will run independent of software control until the registers are changed via software.

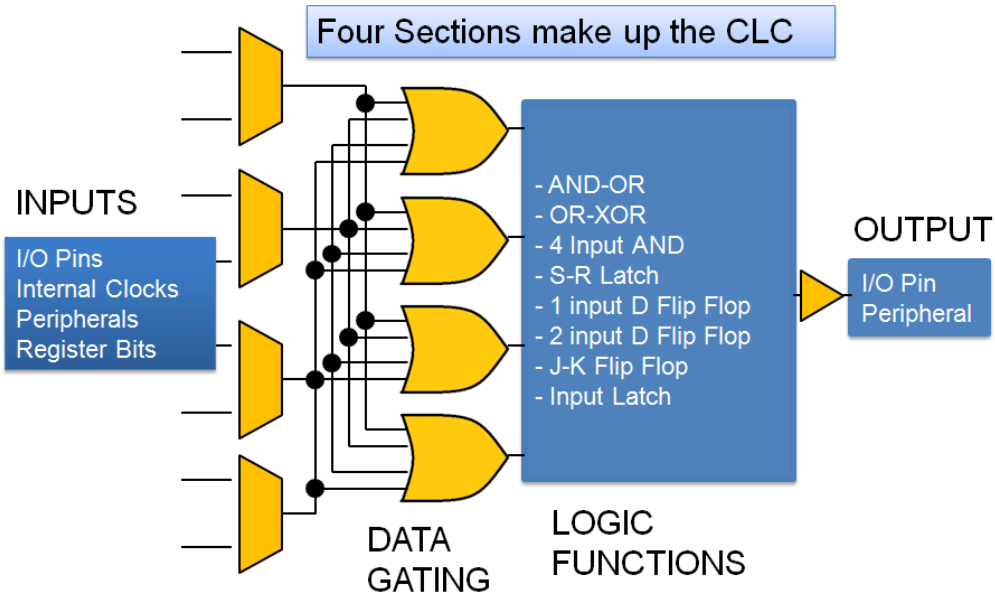
They include:

- **CLCxCON**
- **CLCxSEL0**
- **CLCxSEL1**
- **CLCxGLS0**
- **CLCxGLS1**
- **CLCxGLS2**
- **CLCxGLS3**
- **CLCxPOL**

A PIC Device can have multiple CLC's so each CLC module has its own set of 8 registers. The x in the register names above represent the CLC number (i.e. CLC1 uses the CLC1CON register).

To simplify the setup, the CLC can be broken down into four sections that need to be configured.
They include:

- Inputs
- Data Gating
- Logic Function
- Output Setting



Inputs

Inputs can come from 8 to 16 different sources, depending on the PIC device, and from this list up to four can be chosen to feed the data gating section.
They can include:

- I/O pins
- Internal Clock outputs
- Peripherals outputs
- Register Bits

The inputs are selected by bits in the **CLCxSEL0** and **CLCxSEL1** registers.

Each input has an associated 3-bit code that is placed in the CLCxSEL registers to enable the input.

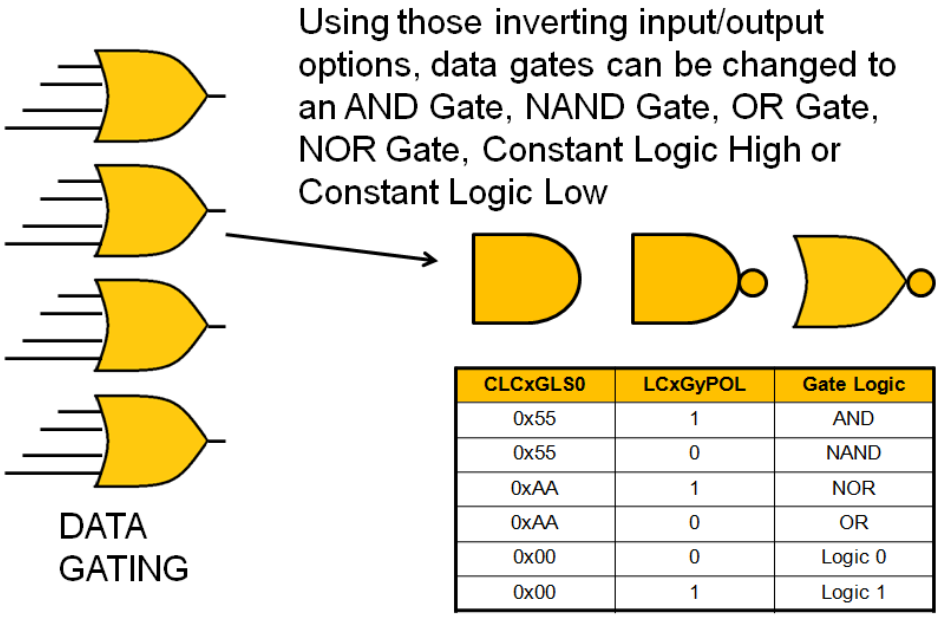
CLC 1 Input	Source
CLC1IN[0] CLC1IN[1]	CLC1IN0 PIN CLC1IN1 PIN
CLC1IN[2] CLC1IN[3]	SYNCC1OUT SYNCC2OUT
CLC1IN[4] CLC1IN[5]	Fosc TMR0IF
CLC1IN[6] CLC1IN[7]	TMR1IF TMR2 = PR2
CLC1IN[8] CLC1IN[9]	lc1_out lc2_out
CLC1IN[10] CLC1IN[11]	lc3_out lc4_out
CLC1IN[12] CLC1IN[13]	NCO1OUT HFINTOSC
CLC1IN[14] CLC1IN[15]	PWM3OUT PWM4OUT

Data Gating

The Data Gating section has four logic gates that need to be setup. This requires five separate registers to be setup. The configure the inverted or non-iverted connection from the inputs that control the CLC peripheral. The five registers include:

- **CLCxGLS0**
- **CLCxGLS1**
- **CLCxGLS2**
- **CLCxGLS3**
- **CLCxPOL**

Each gate starts off as a base OR gate but each input and output can be individually inverted or not inverted.
This allows AND, NAND, OR and NOR gates to be created. The gates can also be setup to drive a constant 1 or 0 logic level.



CLCxGLS0	LCxGyPOL	Gate Logic
0x55	1	AND
0x55	0	NAND
0xAA	1	NOR
0xAA	0	OR
0x00	0	Logic 0
0x00	1	Logic 1

Each input to a data gate has a pair of bits in one of the **CLCxGLSx** registers. The two bits include a non inverted (T) bit and an inverted (N) bit that need to be setup. If the T bit is set then the input is non-inverted. If the N bit is set then the input is inverted. If both are set to zero then the input is not connected to the gate.

CLC1POL

LC1POL	–	–	–	LC1G4POL	LC1G3POL	LC1G2POL	LC1G1POL
							0

CLC1GLS0

LC1G1D4T	LC1G1D4N	LC1G1D3T	LC1G1D3N	LC1G1D2T	LC1G1D2N	LC1G1D1T	LC1G1D1N
0	1	0	1	0	1	0	1

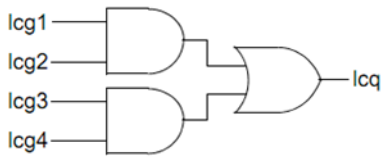
Input 4 Input 3 Input 2 Input 1

The **CLCxPOL** register bit LCxGxPOL bit will invert or non invert the output of the gate.
0 - non inverted
1 - inverted

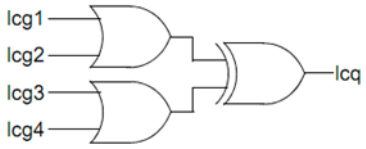
Logic Function

The Logic Function has eight options to choose from. It is selected in the **CLCxCON** register.
Each Logic Function has a 3-bit code associated with it.

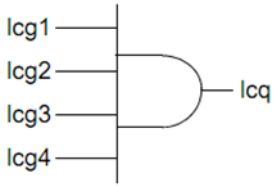
000 = AND – OR



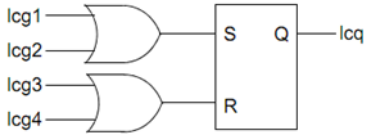
001 = OR – XOR



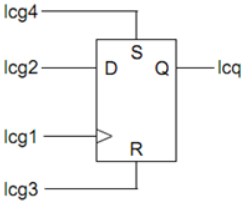
010 = 4-Input AND



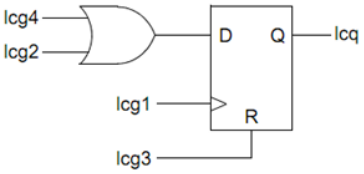
011 = S-R Latch



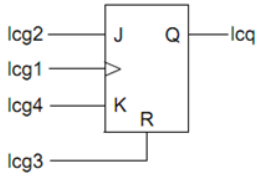
100 = 1-Input D Flip-Flop with S and R



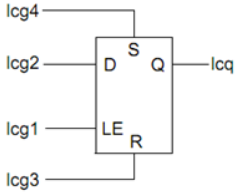
101 = 2-Input D Flip-Flop with R



110 = J-K Flip-Flop with R



111 = 1-Input Transparent Latch with S and R



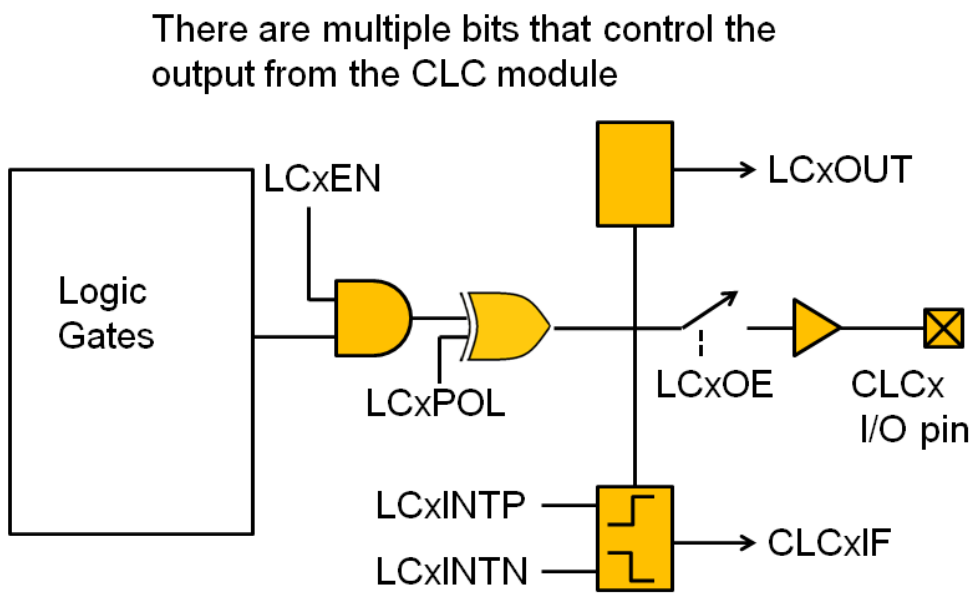
The 3-bit code is set in the CLCxCON register LCxMODE bits to enable the selected Logic Function.

CLCxCON

					LCxMODE < 2 : 0 >		
–	–	–	–	–	1	1	0

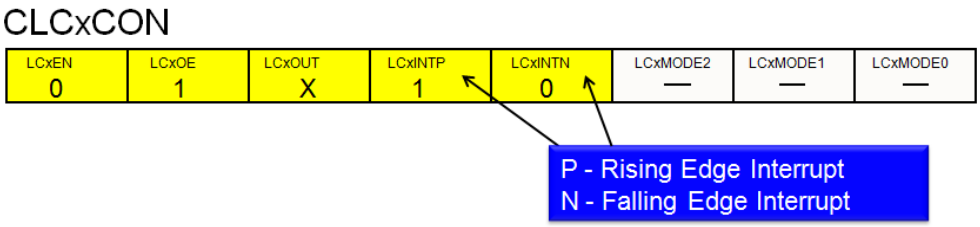
Output

All of the CLC sections reduce down to a single output that can drive an I/O pin, feed another CLC module or internal peripheral or can also trigger an rising or falling edge interrupt.
These various options are setup in the **CLCxCON** and **CLCxPOL** registers.



The bits in the **CLCxCON** register control the output settings.

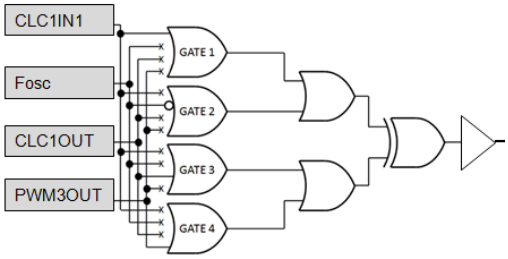
LCxEN – CLC module enable bit (1 - CLC On, 0 - Off)
LCxOE – Output enable bit (1 – Enable, 0 – Disable)
LCxOUT - Internally monitor output via software (Read Only Bit)
LCxINTP – Rising Edge interrupt enable (1-CLCxIF set on Rising Edge)
LCxINTN – Falling Edge interrupt enable (1-CLCxIF set on Falling Edge)



CLC Example

Here is a simple example that shows the eight registers setup in software to create the CLC setup shown in the picture.

The example below shows a setup for the CLC1 module. The eight register settings are shown for this example in a format for the XC8 compiler.




```
// CLC 1 Setup
CLC1SEL0 = 0x01;   // CLC1IN1 Pin, Fosc Inputs
CLC1SEL1 = 0x02;   // CLC1OUT, PWM3OUT Inputs
CLC1GLS0 = 0x01;   // Input 1 not inverted
CLC1GLS1 = 0x04;   // Input 2 inverted
CLC1GLS2 = 0x20;   // Input 3 not inverted
CLC1GLS3 = 0x80;   // Input 4 not inverted
CLC1POL  = 0x00;   // Output of CLC1 is not inverted
CLC1CON = 0xD2;   // Enable OR-XOR, Rising Edge Interrupt, Output Pin Enabled, CLC enabled
```

CLC Designer Tool

The **CLC Designer Tool** is a GUI based tool that you can download for free to make creating the CLC structure much easier. Through a series of setup options the tool will automatically output the eight register settings in C or Assembly language code format so you can include it in your MPLAB X project. The CLC Designer Tool is part of the MPLAB MCC Software tool